Narrow-Channel Effects in LOCOS-Isolated SOI MOSFETs with Variable Thickness

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Introduction. The continuous trend towards smaller geometries implies the analysis of both short- and narrow-channel effects. Although the narrow channels are of high interest in low-power/low-voltage applications, relatively few and rather contrasting results have, in the past, been reported [1-5]. The narrow-channel effects depend on the isolation technology (MESA, LOCOS, STI), wafer origin (SIMOX, Unibond, etc), device architecture (fully- or partially depleted MOSFETs) and film thickness. In this paper, we attempt to elucidate the narrow-channel effects in fully depleted, LOCOS isolated n-MOSFETs as well as their relationship with other key dimensional effects (short channels and ultra-thin films).

Test Devices. The transistors have been fabricated at LETI using standard Unibond wafers (400 nm thick BOX) and conventional 0.25 nm CMOS technology. The film thickness (from 15 to 50 nm) has been adjusted by sacrificial oxidation in the channel region. The lateral LOCOS isolation was complemented by overdoping the sidewalls. The gate oxide was 4.5 nm thick, the film doping was 5x10^17 cm^-3, the channel width varied from 0.3 to 10 µm, and the effective channel length varied from 0.18 to 10 µm.

Long Channels. Figure 1a shows that the characteristics of 37 nm thick MOSFETs are not apparently affected by the activation of the parasitic edge transistor, which has a higher threshold voltage (V_Te > V_T1). A slight edge conduction becomes visible in 15 nm thick MOSFETs (Fig.1b), where the sidewall doping is more difficult to control and less effective. As a general trend, we note that the threshold voltage decreases in narrower devices (Fig.2). This reverse narrow-channel effect contrasts with the case of MESA-isolated SOI n-MOSFETs [3]. Another difference is that in narrow MESA MOSFETs the role of the back gate is reduced causing an attenuation in interface coupling effects. Since the variations of the front-channel threshold voltage versus back gate bias are parallel in our wide and narrow devices (Fig.3), there is no width-controlled gate-channel coupling. Figure 4 shows that the field-effect mobility decreases in narrow devices, presumably reflecting a degradation of the Si crystal in the thin edges. As a test check, transient effects are used to determine the carrier lifetime as a function of width. Note that the subthreshold slope in the ohmic region of operation does not vary significantly with width. In saturation region (Fig.5), the subthreshold swing of 37 nm thick MOSFETs can drop below 60 mV/decade as a consequence of residual floating body effects. Floating body effects are inhibited in very thin (15 nm) or narrow transistors (where the effective thickness on the edges is very small). We demonstrate that the trends observed in Figs.1-5 can be explained by a model based on the gradual variation, along the width direction, in the structure and parameters of the sidewall-transistor (insert of Fig.6): effective doping, film thickness, gate oxide thickness, interface and oxide quality, silicon crystal orientation and defects. Other competing mechanisms, which have been revealed in narrow SOI MOSFETs (fringing field at the island corners [3], reduced coupling between the front channel and the back interface defects [4], etc [1-5]), do not apply in our case.

Back Channel. In order to confirm our model, we have probed the back channel. Obviously, the edge transistor appears to be more homogeneous, when regarded from the back gate (constant oxide thickness, interface quality, and gate control along the width). A clear edge effect now is observed in Fig.6 and explained by the lowering of the back-channel threshold voltage on the sidewalls (due to a thinner silicon film). The back threshold voltage dependence on channel width and film thickness (Fig.7) is comparable with the front channel behavior.

Short Channels. Charge sharing is responsible for the threshold voltage roll-off and swing degradation. The difference in V_T between long and short channels is slightly accentuated (up to 100 mV, Fig.2) in narrow and ultra-thin devices. But, in 15 nm thick transistors, the overall V_T roll-off is clearly improved. Ultra-thin films are even more attractive in terms of DIBL (Fig.8) and longitudinal fringing fields. Remark that the influence of the width is marginal, as compared to the thickness effect.

Conclusion. Systematic front- and back-gate experiments were performed to reveal and understand a variety of narrow-channel effects. They greatly depend on film thickness, channel length and bias, which implies a global device optimization. Acknowledgements. This work has been performed at the Center for Projects in Advanced Microelectronics (CPMA) in Grenoble. The CPMA is operated by CNRS, LETI, INPG and INSA.
REFERENCES

Fig. 1. Subthreshold characteristics for various widths W and film thicknesses tsi.

Fig. 2. Threshold voltage versus channel width for various transistors.

Fig. 3. Front channel threshold voltage versus back gate bias for various tsi and W.

Fig. 4. Field effect mobility versus channel width for various lengths and thicknesses.

Fig. 5. Front channel swing versus channel width; saturation region, long and short channels, variable thickness.

Fig. 6. Back gate subthreshold characteristics influenced by the parasitic sidewall transistor (shown in the insert).
Fig. 7. Back gate threshold voltage versus channel width for various $t_{si}$ and $L$.

Fig. 8. DIBL versus channel width for 15 nm and 37 nm thick transistors.