# Silicon On Insulator Technology

Sorin Cristoloveanu

Laboratoire de Physique des Composants à Semiconducteurs (UMR CNRS & INPG)
ENSERG, B.P. 257, 38016 Grenoble Cedex 1, France

March 22, 1999

## 1 Introduction

Silicon On Insulator (SOI) technology, more specifically Silicon On Sapphire, was originally invented for the niche of radiation-hard circuits. In the last 20 years, a variety of SOI structures have been conceived with the aim of dielectrically separating, using a buried oxide (Fig. 1b), the active device volume from the silicon substrate [1]. Indeed, in an MOS transistor, only the very top region (0.1–0.2 $\mu$m thick, i.e. less than 0.1 % of the total thickness) of the silicon wafer is useful for electron transport and device operation, whereas the substrate is responsible for detrimental, parasitic effects (Fig. 1a).

More recently, the advent of new SOI materials (Unibond, ITOX) and the explosive growth of portable microelectronic devices have attracted considerable attention on SOI for the fabrication of low-power, low-voltage, and high-frequency CMOS circuits.

The aim of this chapter is to overview the state-of-the-art of SOI technologies, including the material synthesis (section 2), the key advantages of SOI circuits (section 3), the structure and performance of typical devices (section 4), and the operation modes of fully-depleted (section 5) and partially-depleted SOI MOSFETs (section 6). Section 7 is dedicated to short-channel effects. The main challenges that SOI is facing, in order to successfully compete with bulk–Si in the commercial arena, are critically discussed in section 8.

## 2 Fabrication of SOI Wafers

Many techniques, more or less mature and effective, are available for the synthesis of SOI wafers [1].

### 2.1 Silicon on Sapphire

Silicon–On–Sapphire (SOS, Fig. 2a$_1$) is the initial member of SOI family. The epitaxial growth of Si films on $Al_2O_3$ gives rise to small silicon islands that eventually coalesce. The interface transition region contains crystallographic defects due to the lattice mismatch and Al contamination from the substrate. The electrical properties suffer from lateral stress, in-depth inhomogeneity of SOS films, and defective transition layer [2].

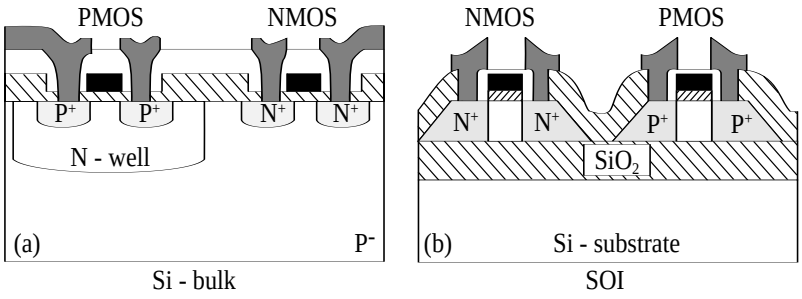


Figure 1: *Basic architecture of MOS transistors in (a) bulk silicon and (b) SOI.*

SOS has recently undergone a significant lifting: larger wafers and thinner films with higher crystal quality. This improvement is achieved by *solid-phase epitaxial regrowth*. Silicon ions are implanted to amorphise the film and erase the memory of damaged lattice and interface. Annealing allows the epitaxial regrowth of the film, starting from the 'seeding' surface towards the Si–$Al_2O_3$ interface. The result is visible in terms of higher carrier mobility and lifetime; 100 nm thick SOS films with good quality have recently been grown on 6" wafers [3].

Thanks to the 'infinite' thickness of the insulator, SOS looks promising for the integration of RF and radiation-hard circuits.

## 2.2 ELO and ZMR

The *Epitaxial Lateral Overgrowth* (ELO) method consists in growing a single-crystal Si film on a seeded and, often, patterned oxide (Fig. $2a_2$). Since the epitaxial growth proceeds in both lateral and vertical directions, ELO process requires a post-epitaxy thinning of the Si film. Alternatively, poly-silicon can be deposited directly on $SiO_2$; subsequently, *Zone Melting Recrystallization* (ZMR) is achieved by scanning high energy sources (lamps, lasers, beams, or strip heaters) across the wafer. ZMR process can be seeded or unseeded; it is basically limited by the lateral extension of single-crystal regions, free from grain subboundaries and associated defects. ELO and ZMR are basic techniques for the integration of 3–D stacked circuits.

## 2.3 FIPOS

The FIPOS method (*Full Isolation by Porous Oxidized Silicon*) makes use of the very large surface-to-volume ratio ($10^3\,cm^2$ per $cm^3$) of porous silicon which is, thereafter, subject to selective oxidation (Fig. $2a_3$). The critical step is the conversion of selected p-type regions of the Si wafer into porous silicon, via anodic reaction. FIPOS may enlighten Si technology because there are prospects, at least from a conceptual viewpoint, for combining electroluminescent porous Si devices with fast SOI–CMOS circuits.

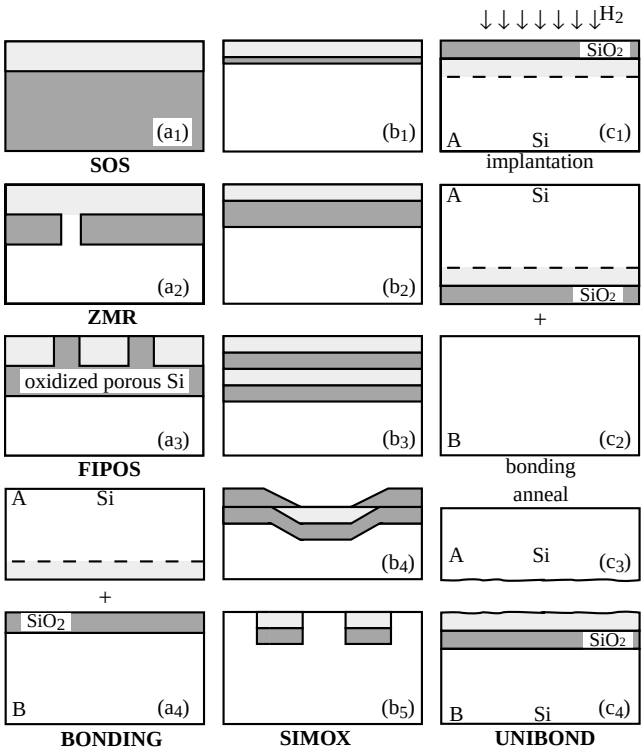


Figure 2: *SOI family: (a) SOS, ZMR, FIPOS, and wafer bonding, (b) SIMOX variants, (c) UNIBOND processing sequence.*

## 2.4 SIMOX

In the last decade, the dominant SOI technology was SIMOX (*Separation by Implantation of Oxygen*). The buried oxide (BOX) is synthesized by internal oxidation during the deep implantation of oxygen ions into a Si wafer. Annealing at high temperature (1320 °C, for 6 hours) is necessary to recover a suitable crystalline quality of the film. High current implanters (100 mA) have been conceived to produce 8" wafers with good thickness uniformity, low defect density (except threading dislocations: $10^4$–$10^6\,\mathrm{cm}^{-2}$), sharp Si-$SiO_2$ interface, robust BOX, and high carrier mobility [4].

The family of SOI structures is presented in Figure 2b:

- Thin and thick Si films fabricated by adjusting the implant energy.
- Low-dose SIMOX: a dose of $4 \times 10^{17}\,\mathrm{O}^+/\mathrm{cm}^2$ and an additional oxygen-rich anneal for enhanced BOX integrity (ITOX process) yield a 0.1 $\mu$m thick BOX (Fig. 2b$_1$).
- Standard SIMOX obtained with $1.8 \times 10^{18}\,\mathrm{O}^+/\mathrm{cm}^2$ implant dose, at 190 keV

and 650 °C; the thicknesses of the Si film and BOX are roughly 0.2 $\mu$m and 0.4 $\mu$m, respectively (Fig. 2b$_2$).

- Double SIMOX (Fig. 2$b_3$), where the Si layer sandwiched between the two oxides can serve for interconnects, wave guiding, additional gates, or electric shielding.
- Laterally-isolated single-transistor islands (Fig. 2b$_4$), formed by implantation through a patterned oxide.
- Interrupted oxides (Fig. 2$b_5$) which can be viewed as SOI regions integrated into a bulk Si wafer.

### 2.5 Wafer Bonding

*Wafer Bonding* (WB) and etch-back stands as a more mature SOI technology. An oxidized wafer is mated to another SOI wafer (Fig. 2a$_4$). The challenge is to drastically thin down one side of the bonded structure in order to reach the targeted thickness of the silicon film. Etch-stop layers can be achieved by doping steps ($P^+/P^-$, P/N) or porous silicon (Eltran process) [5]. The advantage of Wafer Bonding is to provide unlimited combinations of BOX and film thicknesses, whereas its weakness comes from the difficulty to produce ultra-thin films with good uniformity.

### 2.6 UNIBOND

A recent, revolutionary bonding-related process (UNIBOND) uses the deep implantation of hydrogen into an oxidized Si wafer (Fig. 2$c_1$) to generate microcavities and thus circumvent the thinning problem [6]. After bonding wafer $A$ to a second wafer $B$ and subsequent annealing to enhance the bonding strength (Fig. 2$c_2$), the hydrogen-induced microcavities coalesce. The two wafers separate, not at the bonded interface but at a depth defined by the location of hydrogen microcavities. This mechanism, named *Smart–Cut*, results in a rough SOI structure (Fig. 2$c_4$). The process is completed by touch-polishing to erase the surface roughness.

The extraordinary potential of Smart–Cut approach comes from several distinct advantages: (i) the etch-back step is avoided, (ii) the second wafer (Fig. 2$c_3$) being recyclable, UNIBOND is a single-wafer process, (iii) only conventional equipment is needed for mass production, (iv) relatively inexpensive 12" wafers are manufacturable, and (v) the thickness of the silicon film and/or buried oxide can be adjusted to match most device configurations (ultra-thin CMOS or thick-film power transistors and sensors). The defect density in the film is very low, the electrical properties are excellent, and the BOX quality is comparable with that of the original thermal oxide. The Smart–Cut process is adaptable to a variety of materials: SiC or III–V compounds on insulator, silicon on diamond, etc. Smart–Cut can be used to transfer already fabricated bulk-Si CMOS circuits on glass or on other substrates.

## 3 Generic Advantages of SOI

SOI circuits consist of single-device islands dielectrically isolated from each other and from the underlying substrate (Fig. 1b). The lateral isolation offers more compact design and simplified technology than in bulk silicon: there is no need of wells or interdevice trenches. In addition, the vertical isolation renders the *latch-up* mechanisms impossible.

The source and drain regions extend down to the buried oxide, thus the junction surface is minimized. This implies reduced leakage currents and junction capacitances which further translates in improved speed, lower power dissipation, and wider temperature range of operation.

The limited extension of drain and source regions allows SOI devices to be less affected by short-channel effects, originated from 'charge sharing' between gate and junctions. Besides the outstanding tolerance of transient radiation effects, SOI MOSFETs experience a lower electric-field peak than in bulk Si and are potentially more immune to hot carrier damage.

It is in the highly competitive domain of LV/LP circuits, operated with one-battery supply (0.9–1.5 V), that SOI can express its entire potential. A small gate voltage gap is suited to switch a transistor from off- to on-state. SOI offers the possibility to achieve a quasi-ideal subthreshold slope (60 mV/decade at room temperature), hence a threshold voltage shrinked below 0.3 V. Low leakage currents limit the *static* power dissipation, as compared to bulk Si, whereas the *dynamic* power dissipation is minimized by the combined effects of low parasitic capacitances and reduced voltage supply.

Two arguments can be given to outline unequivocally the advantage of SOI over bulk Si:

- Operation at similar *voltage* consistently shows about 30 % increase in performance, whereas operation at similar *low-power* dissipation yields as much as 300 % performance gain in SOI. It is believed, at least in the SOI community, that SOI circuits of generation ($n$) and bulk-Si circuits from the *next* generation ($n+1$) perform comparably.
- Bulk Si technology does attempt to mimic a number of features that are natural in SOI: the double-gate configuration is reproduced by processing surrounded-gate vertical MOSFETs on bulk Si, full depletion is approached by tailoring a low-high step doping, and the dynamic-threshold operation is borrowed from SOI.

The problem for SOI is that such an enthusiastic list of merits did not perturb the fantastic progress and authority of bulk Si technology. There was no room or need so far for an alternative technology such as SOI. However, the SOI community keeps confident that the SOI advantages together with the predictable approach of bulk–Si limits will be enough for SOI to succeed soon.

# 4 SOI Devices

## 4.1 CMOS Circuits

High performance SOI CMOS circuits, compatible with LV/LP and high speed ULSI applications have been repeatedly demonstrated on submicron devices. Quarter-micron ring oscillators showed delay times of 14 ps/stage at 1.5 V [7] and of 45 ps/stage at 1 V [8]. PLL operated at 2.5 V and 4 GHz dissipate 19 mW only [8]. Microwave SOS MOSFETs, with T–gate configuration, had 66 MHz maximum frequency and low noise figure [3].

More complex SOI circuits, with direct impact on mainstream microelectronics, have also been fabricated: 0.5 V–200 MHz microprocessor [9], 4 Mbit SRAM [10], 16 Mbit and 1 Gbit DRAM [11], etc [1, 12]. Several companies (IBM, Motorola,

Sharp) have announced the imminent commercial deployment of 'SOI–enhanced' PC processors and mobile communication devices.

CMOS SOI circuits show capability of successful operation at temperatures higher than 300 °C: the leakage currents are much smaller and the threshold voltage is less temperature-sensitive ($\approx 0.5\,\mathrm{mV/°C}$ for fully depleted MOSFETs) than in bulk Si [13]. In addition, many SOI circuits are radiation-hard, able to sustain doses above 10 Mrad.

## 4.2 Bipolar Transistors

As a consequence of the small film thickness, most of the bipolar transistors have lateral configuration. The implementation of BiCMOS technology on SOI has resulted in devices with a cut-off frequency above 27 GHz [14]. Hybrid MOS–bipolar transistors with increased current drive and transconductance are formed by connecting the gate to the floating body (or base): the MOSFET action governs in strong inversion whereas, in weak inversion, the bipolar current prevails [12].

Vertical bipolar transistors have been processed in thick-film SOI (wafer bonding or epitaxial growth over SIMOX). An elegant solution for thin-film SOI is to replace the buried collector by an inversion layer activated by the back gate [12].

## 4.3 High Voltage Devices

Lateral Double–Diffused MOSFETs (DMOS), with long drift region, were fabricated on SIMOX and showed 90 V–1.3 A capability [15]. Vertical DMOS can be accommodated in thicker wafer-bonding SOI.

SIMOX process offers the possibility to synthesize locally a buried oxide ('interrupted' SIMOX, Fig. $2b_5$). Therefore, a vertical power device (DMOS, IGBT, UMOS, etc), located in the bulk region of the wafer, can be controlled by a low-power CMOS/SOI circuit (Fig. 3a). A variant of this concept is the 'mezzanine' structure, which served for the fabrication of a 600 V/25 A smart-power device [16]. Double SIMOX (Fig. $2b_3$) has also been used to combine a power MOSFET, with a double-shielded high-voltage lateral CMOS and an intelligent low-voltage CMOS circuit [17].

## 4.4 Innovative Devices

Most innovative devices make use of special SOI features, including the possibility to (i) combine bulk Si and SOI on a single chip (Fig. 3a), (ii) adjust the thickness of the Si overlay and buried oxide, and (iii) implement additional gates in the buried oxide (Fig. 3b), by ELO process or by local oxidation of the sandwiched Si layer in double SIMOX (Fig. $2b_3$).

SOI is an ideal material for microsensors because the Si/BOX interface gives a perfect etch-stop mark, making it possible to fabricate very thin membranes (Fig. 3c). Transducers for detection of pressure, acceleration, gas flow, temperature, radiation, magnetic field, etc, have successfully been integrated on SOI [1, 16].

The feasibility of 3–dimensional circuits has been demonstrated on ZMR structures. For example, an image-signal processor is organized in three levels: photodiode arrays in the upper SOI layer, fast A/D converters in the intermediate SOI layer, and arithmetic units and shift registers in the bottom bulk Si level [18].

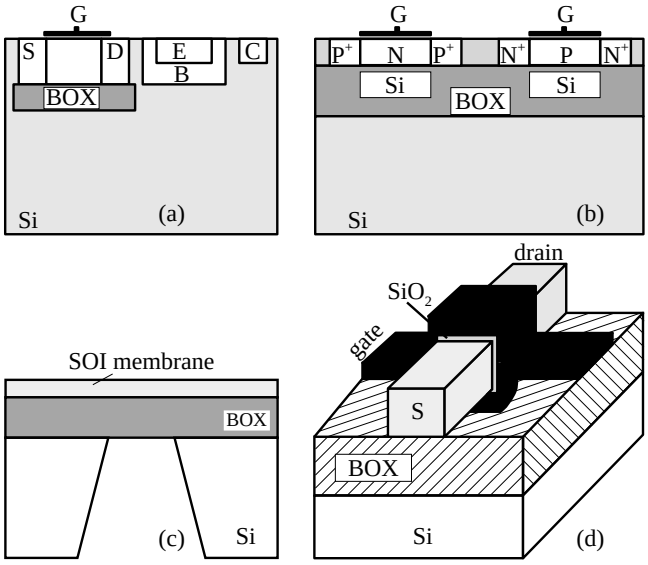


Figure 3: *Examples of innovative SOI devices: (a) combined bipolar (or high power) bulk-Si transistor with low-voltage SOI CMOS circuits, (b) dual-gate transistors, (c) pressure sensor, and (d) Gate–All–Around (GAA) MOSFET.*

The *Gate All–Around* (GAA) transistor of Figure 3d, based on the concept of volume inversion, is fabricated by etching a cavity into the BOX and wrapping the oxidized transistor body into a poly-Si gate [12]. Similar devices are Delta transistor [19] and various double-gate MOSFETs.

The family of SOI devices also includes optical waveguides and modulators, microwave transistors integrated on high resistivity SIMOX, twin-gate MOSFETs, and other exotic devices [1, 12]. They are not belonging to *science fiction*: the devices have already been demonstrated in terms of technology and functionality ... even if most people still do not believe that they can operate indeed.

# 5 Fully–Depleted SOI Transistors

In SOI MOSFETs (Fig. 1b), inversion channels can be activated at both the front Si–$SiO_2$ interface (via gate modulation $V_{G_1}$) and back Si–BOX interface (via substrate, back-gate bias $V_{G_2}$).

*Full depletion* means that the depletion region covers the whole transistor body. The depletion charge is constant and cannot extend according to the gate bias. A better coupling develops between the gate bias and the inversion charge, leading to enhanced drain current. In addition, the front- and back-surface potentials become coupled too. The coupling factor is roughly equal to the thickness ratio between gate oxide and buried oxide. The electrical characteristics of one channel vary remarkably with the bias applied to the opposite gate. Due to *interface coupling*, the front-gate

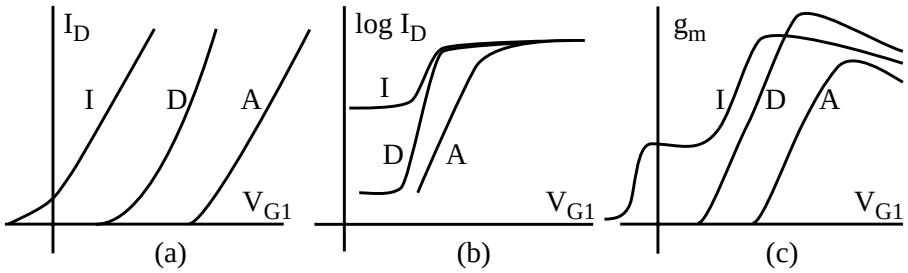


Figure 4: *Generic front-channel characteristics of a fully-depleted n-channel SOI MOSFET for accumulation (A), depletion (D), and inversion (I) at the back interface: (a) $I_D(V_{G_1})$ curves in strong inversion, (b) $\log I_D(V_{G_1})$ curves in weak inversion, and (c) transconductance $g_m(V_{G_1})$ curves.*

measurements are all reminiscent of the back gate bias and quality of the buried oxide and interface.

Totally new $I_D(V_G)$ relations apply to fully-depleted SOI–MOSFETs whose complex behavior is controlled by both gate biases. The typical characteristics of the front-channel transistor are schematically illustrated in Figure 4, for three distinct bias conditions of the back interface (inversion, depletion, and accumulation), and will be explained next.

## 5.1 Threshold Voltage

The lateral shift of $I_D(V_G)$ curves (Fig. 4a) is explained by the linear variation of the front-channel threshold voltage, $V_{T_1}^{dep}$, with back gate bias. This *potential coupling* causes $V_{T_1}^{dep}$ to decrease linearly, with increasing $V_{G_2}$, between two plateaus corresponding respectively to accumulation and inversion at the back interface [20]:

$$V_{T_1}^{dep} = V_{T_1}^{acc} - \frac{C_{si}C_{ox_2}\left(V_{G_2} - V_{G_2}^{acc}\right)}{C_{ox_1}(C_{ox_2} + C_{si} + C_{it_2})} \tag{1}$$

where $V_{T_1}^{acc}$ is the threshold voltage when the back interface is accumulated

$$V_{T_1}^{acc} = \Phi_{fb_1} + \frac{C_{ox_1} + C_{si} + C_{it_1}}{C_{ox_1}} 2\Phi_F - \frac{Q_{si}}{2C_{ox_1}} \tag{2}$$

and $V_{G_2}^{acc}$ is given by

$$V_{G_2}^{acc} = \Phi_{fb_2} - \frac{C_{si}}{C_{ox_2}} 2\Phi_F - \frac{Q_{si}}{2C_{ox_2}} \tag{3}$$

In the above equations, $C_{si}$, $C_{ox}$ $C_{it}$ are the capacitances of the fully-depleted film, oxide, and interface traps, respectively; $Q_{si}$ is the depletion charge, $\Phi_F$ is the Fermi potential, and $\Phi_{fb}$ is the flat-band potential. The subscripts 1 and 2 hold for the front or the back channel parameters and can be interchanged to account for the variation of the back-channel threshold voltage $V_{T_2}$ with $V_{G_1}$.

The difference between the two plateaus, $\Delta V_{T_1} = (C_{si}/C_{ox_1})2\Phi_F$, slightly depends on doping, whereas the slope does not. We must insist on the polyvalence of

Eqs.(1–3) as compared to the simple case of bulk Si MOSFETs (or partially-depleted MOSFETs), where

$$V_{T_1} = \Phi_{fb_1} + \left(1 + \frac{C_{it_1}}{C_{ox_1}}\right) 2\Phi_F + \frac{\sqrt{4q\epsilon_{si}N_A\Phi_F}}{C_{ox_1}} \tag{4}$$

The extension to p-channels or accumulation-mode SOI–MOSFETs is also straightforward [1].

In fully-depleted MOSFETs, the threshold voltage decreases in thinner films (i.e reduced depletion charge), until quantum effects arise and lead to the formation of a 2–D subband system. In ultra-thin films ($t_{si} \leq 10\,\text{nm}$), the separation between the ground state and the bottom of the conduction band increases with reducing thickness: a $V_T$ rebound is then observed [21].

## 5.2 Subthreshold Slope

For depletion at the back interface, the subthreshold slope (Fig. 4b) is very steep and the subthreshold *swing* $S$ is given by [22]:

$$S_1^{dep} = 2.3\frac{kT}{q}\left(1 + \frac{C_{it_1}}{C_{ox_1}} + \alpha_1\frac{C_{si}}{C_{ox_1}}\right) \tag{5}$$

The interface coupling coefficient $\alpha_1$

$$\alpha_1 = \frac{C_{ox_2} + C_{it_2}}{C_{si} + C_{ox_2} + C_{it_2}} < 1 \tag{6}$$

accounts for the influence of back interface traps $C_{it_2}$ and buried oxide thickness $C_{ox_2}$ on the front channel current [22].

In the ideal case, where $C_{it_{1,2}} \simeq 0$ and the buried oxide is much thicker than both the film and the gate oxide (i.e $\alpha_1 \simeq 0$), the swing approaches the theoretical limit $S_1^{dep} \simeq 60\,\text{mV/decade}$ at 300 K. Accumulation at the back interface does decouple the front inversion channel from back interface defects but, in turn, makes $\alpha_1$ tend to unity (as in bulk–Si or partially-depleted MOSFETs), causing an overall degradation of the swing.

It is worth noting that the above simplified analysis and equations are valid only when the buried oxide is thick enough such as substrate effects occurring underneath the BOX can be overlooked. The capacitances of the BOX and Si substrate are connected in series. Therefore, the swing may depend, essentially for thin buried oxides, on the density of traps and surface charge (accumulation, depletion, or inversion) at the *third* interface: BOX–Si substrate. The general trend is that the subthreshold slope improves for thinner silicon films and thicker buried oxides.

## 5.3 Transconductance

For strong inversion and ohmic region of operation, the front-channel drain current and transconductance are given by

$$I_D = \frac{C_{ox_1}WV_D}{L} \cdot \frac{\mu_1}{1 + \theta_1(V_{G_1} - V_{T_1}(V_{G_2}))} \cdot (V_{G_1} - V_{T_1}(V_{G_2})) \tag{7}$$

$$g_{m_1} = \frac{C_{ox_1}WV_D}{L} \cdot \frac{\mu_1}{[1 + \theta_1(V_{G_1} - V_{T_1}(V_{G_2}))]^2} \tag{8}$$

where $\mu_1$ is the mobility of front channel carriers, and $\theta_1$ is the mobility attenuation coefficient.

The complexity of the transconductance curves in fully depleted MOSFETs (Fig. 4c) is explained by the influence of the back gate bias via $V_{T_1}(V_{G_2})$. The effective mobility and transconductance peak are maximum for depletion at the back interface, due to combined effects of reduced vertical field and series resistances.

An unusual feature is the distortion of the transconductance (curve I, Fig. 4c) which reflects the possible activation of the back channel, far before the inversion charge build-up is completed at the front channel [23]. While the front interface is still depleted, increasing $V_{G_1}$ reduces the back threshold voltage and eventually opens the *back* channel, The plateau of the front-channel transconductance (Fig. 4c) can be used to derive directly the back-channel mobility.

### 5.4 Volume Inversion

In thin and low-doped films, the simultaneous activation of front and back channels induces by continuity (*i.e charge coupling*) the onset of *volume inversion* [24]. Unknown in bulk Si, this effect enables the inversion charge to cover the whole film. Self-consistent solutions of Poisson and Schrödinger equations indicate that the maximum density of the inversion charge is reached in the middle of the film. This results in increased current drive and transconductance, attenuated influence of interface defects (traps, fixed charges, roughness), and reduced $1/f$ noise.

Double-gate MOSFETs (*DELTA* and *GAA* transistors), designed to take full advantage from volume inversion, also benefit from reduced short-channel effects ($V_T$ drop, punch-through, DIBL, hot-carrier injection, etc), and are therefore very attractive, if not unique, devices for down scaling below 30 nm gate length.

### 5.5 Defect Coupling

In fully-depleted MOSFETs, carriers flowing at one interface may sense the presence of defects located at the opposite interface. *Defect coupling* is observed as an apparent degradation of the front channel properties, which is actually induced by the buried oxide damage. This unusual mechanism is notorious after back interface degradation via radiation or hot-carrier injection (see also Fig. 7 in Section 7).

## 6 Partially–Depleted SOI Transistors

In partially-depleted SOI MOSFETs, the depletion charge controlled by one or both gates does not extend from an interface to the other. A neutral region subsists and, therefore, the interface coupling effects are disabled. When the body is grounded (via independent body contacts or body-source ties), partially-depleted SOI transistors behave very much alike bulk–Si MOSFETs and most of the standard $I_D(V_G, V_D)$ equations and design concepts apply. If body contacts are not supplied, so-called *floating-body* effects arise, leading to detrimental consequences which will be explained next.

The *kink* effect is due to majority carriers, generated by impact ionization, which collect in the transistor body. The body potential is raised which reduces the threshold voltage. This feedback gives rise to extra drain current (kink) in $I_D(V_D)$ characteristics (Fig. 5a) which is annoying in analog circuits.

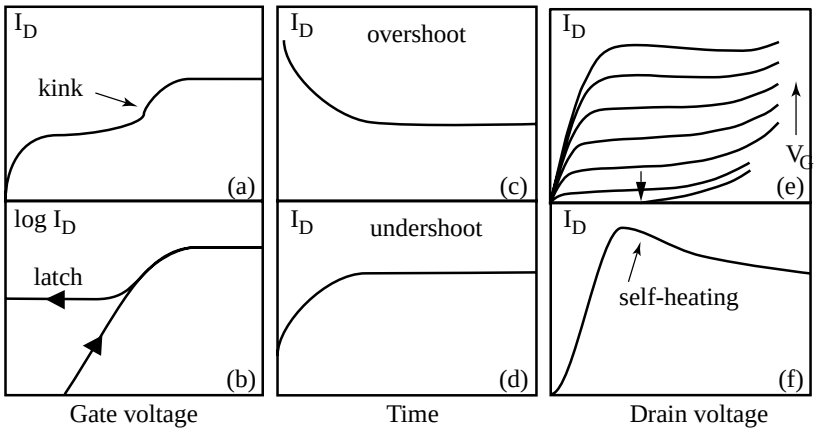


Figure 5: *Parasitic effects in partially-depleted SOI MOSFETs: (a) kink in $I_D(V_D)$ curves, (b) latch in $I_D(V_G)$ curves, (c)drain current overshoot, (d) current undershoot, (e) premature breakdown, and (f) self-heating.*

In weak inversion and for high drain bias, a similar positive feedback (increased inversion charge $\rightarrow$ more impact ionization $\rightarrow$ body charging $\rightarrow$ threshold voltage lowering) is responsible for negative resistance regions, hysteresis in $\log I_D(V_G)$ curves, and eventually latch (loss of gate control, Fig. 5b).

The floating body may also induce transient effects. A drain current *overshoot* is observed when the gate is turned on (Fig. 5c). Majority carriers are expelled from the depletion region and collect in the neutral body increasing the potential. Equilibrium is reached through electron-hole recombination which eliminates the excess majority carriers, making the drain current to decrease gradually with time. A reciprocal *undershoot* occurs when the gate is switched from strong to weak inversion: the current now increases with time (Fig. 5d) as the majority carrier generation allows the depletion depth to shrink gradually. In short-channel MOSFETs, the transient times are dramatically reduced because of the additional contribution of source and drain junctions to establish equilibrium.

An obvious solution to alleviate floating-body effects is to sacrifice chip space for designing body contacts. The problem is that, in ultra-thin films with large sheet resistance, the body contacts are far from being ideal. Their intrinsic resistance does not allow the body to be perfectly grounded and may generate additional noise. A floating body is then preferable to a poor body contact.

An exciting partially-depleted device is the *dynamic-threshold* DT–MOS transistor. It is simply configured by interconnecting the gate and the body. As the gate voltage increases in weak inversion, the simultaneous raise in body potential makes the threshold voltage to decrease. DT–MOSFETs achieve perfect gate-charge coupling, maximum subthreshold slope, and enhanced current, which are attractive features for LV/LP circuits.

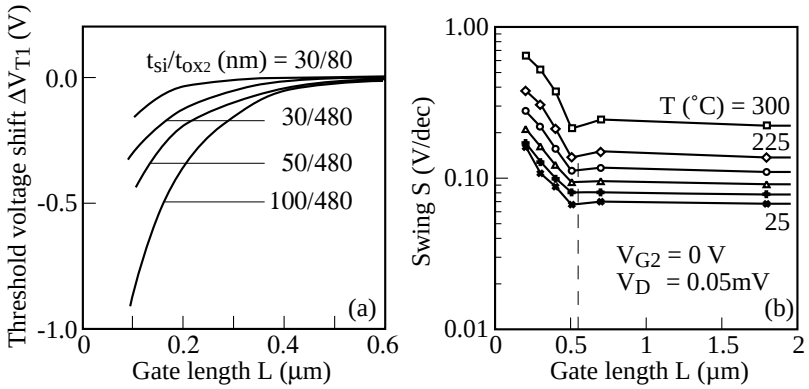


Figure 6: *Typical short-channel effects in fully-depleted SOI MOSFETs: (a) threshold voltage roll-off for different thicknesses of film and buried oxide [26] and (b) subthreshold swing degradation below 0.2 μm channel length for various temperatures [13]*

.

# 7 Short–Channel Effects

In both fully- and partially-depleted MOSFETs with submicron length, the source-body junction can easily be turned on. The inherent activation of the lateral bipolar transistor has favorable (extra current flow in the body) or detrimental (premature breakdown, Fig. 5e) consequences. The breakdown voltage is evaluated near threshold, where the bipolar action prevails. The breakdown voltage is especially lowered for n-channels, shorter devices, thinner films, and higher temperatures. As expected, the impact ionization rate and related floating-body effects are attenuated at high temperature. However, the bipolar gain increases dramatically with temperature and accentuates the bipolar action: lower breakdown and latch voltages [13].

Another concern is *self-heating*, induced by the power dissipation of short-channel MOSFETs and exacerbated by the poor thermal conductivity of the surrounding $SiO_2$ layers. Self-heating is responsible for mobility degradation, threshold voltage shift, and negative differential conductance shown in Figure 5f. The temperature raise can exceed 100–150° C in SOI, which is far more than in bulk Si [25]. Electromigration may even be initiated by the resulting increase in interconnect temperature. Thin buried oxides ($\leq$ 100 nm) and thicker Si films ($\geq$ 100 nm) are suitable when self-heating becomes a major issue.

A familiar short-channel effect is the threshold voltage roll-off due to charge sharing between the gate and source and drain terminals. The key parameters in SOI are the doping level, film thickness, and BOX thickness [26]. Ultra-thin, fully-depleted MOSFETs show improved performance in terms of both $V_T$ roll-off and drain-induced barrier lowering (DIBL) as compared to partially-depleted SOI or bulk Si transistors (Fig. 6a) [27]. The worst case happens when the film thickness corresponds to the transition between full and partial depletion. An additional origin of $V_T$ roll-off in fully-depleted MOSFETs is the field penetration into the buried oxide. An obvious solution is again the use of relatively thin buried oxides.

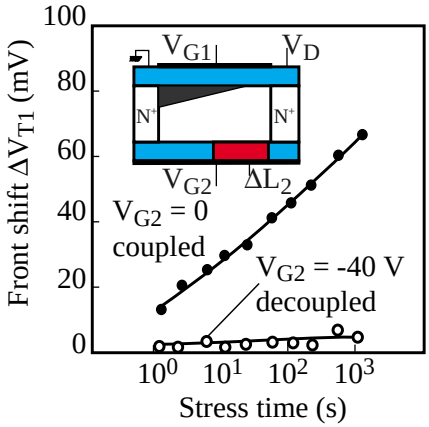


Figure 7: *Front-channel threshold voltage shift during back-channel stress in a SIMOX MOSFET [28]. The apparent degradation of the gate oxide disappears when the stress-induced defects in the buried oxide are masked by interface accumulation ($V_{G_2} = -40$ V).*

A degradation of the subthreshold swing is observed in very short ($L \leq 0.3$–$0.5\,\mu$m), fully-depleted MOSFETs (Fig. 6b). Two effects are involved: (i) conventional charge sharing, and (ii) a surprising non-uniform coupling effect. We have seen that the subthreshold swing is minimum for depletion and increases for inversion at the back interface. In very short transistors, the lateral profile of the back interface potential can be highly inhomogeneous: from depletion in the middle of the channel to weak inversion near the channel ends, due to the proximity of source and drain regions. This localized weak inversion region explains the degradation of the swing [13].

The transconductance is obviously improved in deep submicron transistors. Velocity saturation occurs as in bulk silicon. The main short-channel limitation of the transconductance comes from series resistance effects.

The lifetime of submicron MOSFETs is affected by hot-carrier injection into the gate oxide(s). The degradation mechanisms are more complex in SOI than in bulk Si, due to the presence of two oxides, two channels and related coupling mechanisms. For example, in Fig. 7, the front-channel threshold voltage is monitored during back channel stress. The shift $\Delta V_{T_1}$, measured for $V_{G_2} = 0$ (depleted back-interface), would imply that many defects are being generated at the front interface. Such a conclusion is totally negated by measurements performed with $V_{G_2} = -40$ V: the influence of buried-oxide defects now is masked by the accumulation layer and indeed the apparent front-interface damage disappears ($\Delta V_{T_1} \simeq 0$) [28].

In n-channels, the defects are created at the interface where the electrons flow; exceptionally, injection into the opposite interface may arise when the transistor is biased in the breakdown region. Although the device lifetime is relatively similar in bulk Si and SOI, the influence of stressing bias is different: SOI MOSFETs degrade less than bulk Si MOSFETs for $V_G \simeq V_D/2$ (i.e for maximum substrate current) and more for $V_G \simeq V_T$ (i.e enhanced hole injection). The device aging is accelerated by

accumulating the back interface [28].

In p-channels, the key mechanism involves the electrons generated by front-channel impact ionization, which become trapped into the buried oxide. An apparent degradation of the front interface again occurs via coupling [28].

# 8 SOI Challenges

SOI stands already as a pretty mature technology. However, there are still serious challenges in various domains—fundamental and device physics, technology, device modeling, and circuit design—before SOI will become fully competitive in the commercial market.

The minimum dimensions so far achieved for SOI MOSFETs are: 70 nm length, 10 nm width (quantum wires), and 1–2 nm thickness [21]. When these features will be cumulative in a single transistor, the body volume ($\leq 10^{-18}\,\mathrm{cm}^3$ !) will contain $10^4$–$10^5$ silicon atoms and 0–1 defects. The body doping ($10^{17}$–$10^{18}\,\mathrm{cm}^{-3}$) will be provided by a unique impurity, whose location may become important. Moreover, quantum transport phenomena are already being observed in ultra-thin SOI transistors. It is clear that new physical concepts, ideas, and modeling tools will be needed to account for minimum-size mechanisms in order to take advantage of them.

As far as the technology is concerned, a primary challenge is the mass production of SOI wafers with large diameter ($\geq 12$"), low defect content, and reasonable cost (2–3 times higher than for bulk Si wafers). The thickness uniformity of the silicon layer is especially important for fully-depleted MOSFETs because it governs the fluctuations of the threshold voltage. It is predictable that several SOI technologies will not survive, except for special niches.

There is a demand for appropriate characterization techniques, either imported from other semiconductors or entirely conceived for SOI [1]. Such a pure SOI technique is the pseudo–MOS transistor ($\Psi$–MOSFET) [29]. Ironically, it behaves very much alike the MOS device that Shockley attempted to demonstrate 50 years ago but, at that time, he didn't have the chance to know about SOI. The inset of Figure 8 shows that the Si substrate is biased as a gate and induces a conduction channel (inversion or accumulation) at the film-oxide interface. Source and drain probes are used to measure $I_D(V_G)$ characteristics. The $\Psi$–MOSFET does not require any processing, hence valuable information is directly available: quality of the film, interface and oxide, electron/hole mobilities and lifetime.

Full CMOS processing must address typical SOI requirements such as the series resistance reduction in ultra-thin MOSFETs (via local film oxidation, elevated source and drain structures, etc), the lowering of the source-body barrier by source engineering (silicidation, Si–Ge, etc), the control of the parasitic bipolar transistor, and the limitation of self-heating effects. It is now clear that the best of SOI is certainly not achievable by simply using a very good bulk-Si technology. For example, double-gate SOI MOSFETs deserve special processing and design.

According to process engineers and circuit designers, partially-depleted SOI MOSFETs are more user friendly as they maintain the flavor of bulk–Si technology. On the other hand, fully-depleted transistors have superior capability; they need to be domesticated in order to become more tolerant to short-channel effects. A possible solution, which requires further investigation, is the incorporation of a ground plane in the buried oxide.

Advanced modeling is requested for correct transcription of the transistor behaviour

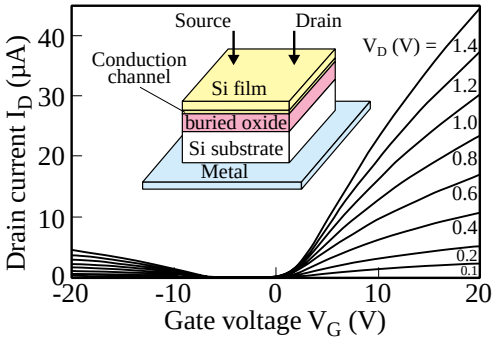


Figure 8: *Pseudo–MOSFET transistor and $I_D(V_G)$ characteristics in SOI.*

including the transient effects due to body charging and discharging, floating body mechanisms, bipolar transistor, dual gate operation, quantum effects, self-heating, and short-channel limitations. Based on such physical models, compact models should then be conceived for customized simulation and design.

It is obvious that SOI does need SOI–dedicated CAD libraries. This implies a substantial amount of work which, in turn, will guarantee that the advantages and peculiar constrains of SOI devices are properly accounted for. The optimum configuration of memories, microprocessors, DSP, etc, will most likely be different in SOI as compared to bulk. Not only can SOI afford to combine fully/partially depleted, low/high power, and DT–MOSFETs in a single chip, but also the basic mechanisms of operation differ.

# 9 Conclusion

For the next millennium, SOI offers the opportunity to integrate high performance and/or innovative devices which can push away the present frontiers of the CMOS down-scaling. SOI will play a significant role in the microelectronics future if subsisting problems can be rapidly solved. The short-term prospects of SOI–based microelectronics will also closely depend on the penetration rate of LV/LP SOI circuits into the market. Not only does SOI offer enhanced performance, but also most of SOI disadvantages (self-heating, hot-carriers, early breakdown, etc) tend to disappear for operation at low voltage.

A key challenge is associated with the industrial strategy, which must be oriented to overcome the bulk-Si mono-cultural barrier. Designers, process engineers and managers are extremely busy loading the bulk-Si machine. When, eventually, they will afford to take a careful look at the assets of SOI technology, they will realize the immediate and long-term benefits offered in terms of performance and scaling extensions.

This is so because SOI is not a totally different technology, it is just a metamorphosis of silicon.

## References


[1] S. Cristoloveanu and S.S. Li, "Electrical Characterization of SOI Materials and Devices", *Kluwer*, Norwell (1995).

[2] S. Cristoloveanu, "Silicon films on sapphire", *Rep. Prog. Phys.*, **3**, 327 (1987).

[3] R.A. Johnson, P.R. de la Houssey, C.E. Chang, P–F. Chen, M.E. Wood, G.A. Garcia, I. Lagnado, and P.M. Asbeck, "Advanced thin-film silicon-on-sapphire technology: microwave circuit applications", IEEE Trans. Electron Devices, vol. 45, p. 1047 (1998).

[4] S. Cristoloveanu, "A review of the electrical properties of SIMOX substrates and their impact on device performance", *J. Electrochem. Soc.*, **138**, 3131 (1991).

[5] N. Sato, S. Ishii, S. Matsumura, M. Ito, J. Nakayama, and T. Yonehara, "Reduction of crystalline defects to $50/cm^2$ in epitaxial layers over porous silicon for Eltran", *IEEE Int. SOI Conf.*, Stuart, Florida (1998).

[6] M. Bruel, "Silicon on insulator material technology", *Electronics Lett.*, **31**, 1201 (1995).

[7] J. Chen, S. Parke, J. King, F. Assaderaghi, P. Ko, and C. Hu, "A high-speed SOI technology with 12 ps/18 ps gate delay operating at 5 V/1.5 V", *IEDM Techn. Dig.*, p. 35 (1992).

[8] T. Tsuchiya, T. Ohno and Y. Kado, "Present status and potential of subquarter-micron ultra-thin-film CMOS/SIMOX technology", *SOI Technology and Devices*, Electrochem. Soc., Pennington, p. 401 (1994).

[9] T. Fuse et al, "A 0.5 V 200 MHz 1–stage 32 b ALU using a body bias controlled SOI pass-gate logic", *ISSCC Techn. Digest*, 286 (1997).

[10] D.J. Schepis et al, "A 0.25 $\mu$m CMOS SOI technology and its application to 4 Mb SRAM", *IEDM Techn. Dig.*, 587 (1997).

[11] Y–H. Koh et al, "1 Gigabit SOI DRAM with fully bulk compatible process and body-contacted SOI MOSFET structure", *IEDM Techn. Dig.*, 579 (1997).

[12] J–P. Colinge, "SOI Technology: Materials to VLSI" (2nd ed.), *Kluwer*, Boston (1997).

[13] S. Cristoloveanu and G. Reichert, "Recent advances in SOI materials and device technologies for high temperature", in press (1998).

[14] T. Hiramoto, N. Tamba, M. Yoshida et al, "A 27 GHz double polysilicon bipolar technology on bonded SOI with embedded 58 $\mu m^2$ CMOS memory cell for ECL–CMOS SRAM applications", IEDM Techn. Dig., p. 39 (1992).

[15] O'Connor J. M., Luciani V. K., and Caviglia A. L., "High voltage DMOS power FETs on thin SOI substrates", IEEE Int. SOI CONF. Proc., p. 167 (1990).

[16] H. Vogt, "Advantages and potential of SOI structures for smart sensors", *SOI Technology and Devices*, Electrochem. Soc., Pennington, p. 430 (1994).

[17] Ohno T., Matsumoto S., and Izumi K., "An intelligent power IC with double buried-oxide layers formed by SIMOX technology", IEEE Trans. Electron Devices, vol. 40, p. 2074 (1993).

[18] T. Nishimura, Y. Inoue, K. Sugahara, S. Kusonoki, T. Kumamoto, S. Nakagawa, M. Nakaya, Y. Horiba, and Y. Akasaka, "Three dimensional IC for high performance image signal processor", *IEDM Dig.*, p. 111 (1987).

[19] D. Hisamoto, T. Kaga and E. Takeda, "Impact of the vertical SOI 'DELTA' structure on planar device technology", *IEEE Trans. Electron Dev.*, vol. 38, p. 1419 (1991).

[20] H-K. Lim and J.G. Fossum, "Threshold voltage of thin-film silicon on insulator (SOI) MOSFETs", *IEEE Trans. Electron Dev.*, **30**, 1244 (1983).

[21] Y. Ohmura, T. Ishiyama, M. Shoji and K. Izumi, "Quantum mechanical transport characteristics in ultimately miniaturized MOSFETs/SIMOX", *SOI Technology and Devices*, Electrochem. Soc., Pennington, p. 199 (1996).

[22] B. Mazhari, S. Cristoloveanu, D.E. Ioannou and A.L. Caviglia, "Properties of ultra-thin wafer-bonded silicon on insulator MOSFETs", *IEEE Trans. Electron Dev.*, vol. ED–38, p. 1289 (1991).

[23] T. Ouisse, S. Cristoloveanu, and G. Borel, "Influence of series resistances and interface coupling on the transconductance of fully depleted silicon-on-insulator MOSFETs", *Solid-State Electron.*, vol. 35, p. 141 (1992).

[24] F. Balestra, S. Cristoloveanu, M. Bénachir, J. Brini, and T. Elewa, "Double-gate silicon on insulator transistor with volume inversion: a new device with greatly enhanced performance", *IEEE Electron Device Lett.*, **8**, 410 (1987).

[25] L.T. Su, K.E. Goodson, D.A. Antoniadis, M.I. Flik, and J.E. Chung, "Measurement and modeling of self-heating effects in SOI n–MOSFETs", *IEDM Dig.*, p. 111 (1992).

[26] Y. Ohmura, S. Nakashima, K. Izumi, and T. Ishii, "0.1-$\mu$m-gate, ultra-thin film CMOS device using SIMOX substrate with 80-nm-thick buried oxide layer," IEDM Techn. Dig., p. 675 (1991).

[27] F. Balestra and S. Cristoloveanu, "Special mechanisms in thin-film SOI MOSFETs", *Microelectron. Reliab.*, **37**, 1341 (1997).

[28] S. Cristoloveanu, "Hot-carrier degradation mechanisms in silicon-on-insulator MOSFETs", *Microelectron. Reliab.*, **37**, 1003 (1997).

[29] S. Cristoloveanu and S. Williams, "Point contact pseudo–MOSFET for in-situ characterization of as-grown silicon on insulator wafers", *IEEE Electron Device Lett.*, **13**, 102 (1992).