Recent Advances in SOI Materials and Device Technologies for High Temperature

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Abstract— **The present status of Silicon–On–Insulator (SOI) technologies, structures and devices is reviewed with the aim of demonstrating the attractiveness of SOI for high-temperature applications. The basic MOSFET parameters (leakage current, threshold voltage, carrier mobility and subthreshold swing) are described as a function of temperature up to 300°C. The temperature behavior of more specific SOI mechanisms, induced by the floating body, interface coupling and parasitic bipolar transistor, is also discussed.**

I. Introduction

In MOSFETs, only the top region (0.1–0.2 μm thick) of the silicon wafer is useful for electron transport. SOI structures emerged from the concept of separating the active device overlay from the detrimental influence of the silicon substrate by a buried oxide (Fig. 1). The following are intrinsic advantages of SOI devices [1].

Dielectric isolation. SOI circuits consist of single-device islands, separated from each other (lateral isolation) and from the substrate (vertical isolation). SOI–CMOS circuits are naturally free from latch-up, hence there is no need for sophisticated schemes of trench isolation.

Vertical junctions. The source and drain regions extend to the insulator and only their lateral sides serve as junctions. This yields a substantial reduction in parasitic capacitances, leakage current, and short-channel effects.

Circuit design and processing. The absence of wells and inter-device trenches reduces the number of processing steps and offers, in principle, additional design flexibility for CMOS circuits.

Low voltage/power operation. In thin, fully-depleted SOI transistors, the subthreshold slope is sharper and the leakage current is much lower than in bulk Si. Therefore, the threshold voltage can easily be set around 0.3 V and, for a predefined power consumption, much denser and faster circuits can be integrated on SOI.

High voltage/power operation. The flexibility of SOI structures (variable film and oxide thicknesses, double buried oxide, interrupted oxides, electric shield engineering, etc) makes it more suitable than the isolated bulk-Si technology for the fabrication of high and medium power/voltage devices. Single-chip smart-power circuits can also be integrated by combining a vertical power component, located in the non-SOI section of the chip, with a control low-power SOI circuit.

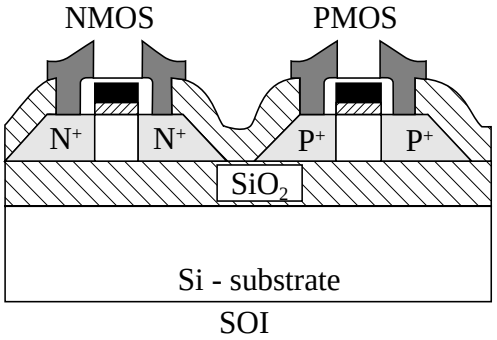

Fig. 1. Generic configuration of CMOS transistors in silicon-on-insulator wafers.

High temperature operation. This paper will demonstrate that CMOS SOI circuits have capability of successful operation at temperatures higher than 250–300 °C, opening a huge range of applications (automotive, avionics, ...). The basic merits of SOI are: no temperature-activated latch-up, much smaller leakage current, and less temperature-sensitive threshold voltage than in bulk Si.

Reliability. The historic motivation for SOI devices was their excellent tolerance of *transient* radiation effects. Logic upsets are greatly reduced since the SOI device volume exposed to radiation-induced carrier generation is 2–3 orders of magnitude smaller than the corresponding volume in bulk Si.

These merits of SOI were not enough to stop the incredible progress of bulk Si technology which has actually delayed the entering of SOI into the commercial arena. There are also internal circumstances which have contributed to inhibit the development of SOI: (i) the

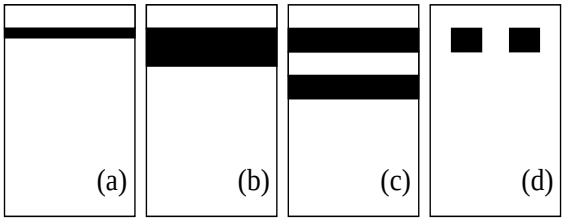

Fig. 2. Typical SIMOX structures: (a) ITOX (lower dose, thin BOX), (b) standard SIMOX, (c) double BOX, (d) interrupted BOX.

uniformity, availability, and cost of SOI wafers must be improved, (ii) specific transistor effects, such as floating body, dynamic transients and interface coupling, require a better understanding and control, (iii) the technology and design of integrated circuits are not fully customized for SOI.

II. Synthesis of SOI Materials

A. SIMOX

The buried oxide (BOX) is synthesized by internal oxidation during the deep implantation of oxygen ions into Si wafers. Typical implantation conditions are $1.8 \times 10^{18}\,O^+/cm^2$, 190 keV, 100 mA, and 650 °C. The thicknesses of the Si overlay and BOX are roughly 200 nm and 380 nm, respectively. Annealing at high temperature (1320 °C, for 6 hours) is necessary to recover the crystalline quality of the film. In commercially available 8" SIMOX wafers, the buried oxide *interfaces* are sharp and uniform [1].

Several SIMOX variants have been explored (Fig. 2): thin and thick films, ultra-thin BOX, interrupted oxide. In the double SIMOX structure (Fig. 2c), fabricated by high/low dose implants, the silicon layer sandwiched between the two oxides is useful for interconnects, electrical shielding, or optical waveguides. Recent attention is given to the low-dose material (ITOX), with ultra-thin Si film (< 100 nm) and BOX (80–100 nm), since heat dissipation of integrated circuits and short-channel effects are improved.

B. Wafer Bonding

Wafer Bonding (WB) technology provides undamaged crystal quality and a wide range of thicknesses for both the SOI film and the BOX. The generic processing steps are [2]: (i) mating two oxidized silicon wafers together, (ii) annealing to increase the bonding strength, and (iii) thinning one of the two wafers by grinding and etching. The latter step is more critical as it needs an etch-stop layer. This explains the difficulty in manufacturing ultrathin and uniform Si films. A recently developed plasma-assisted chemical etching method provides 100 nm SOI films with good uniformity

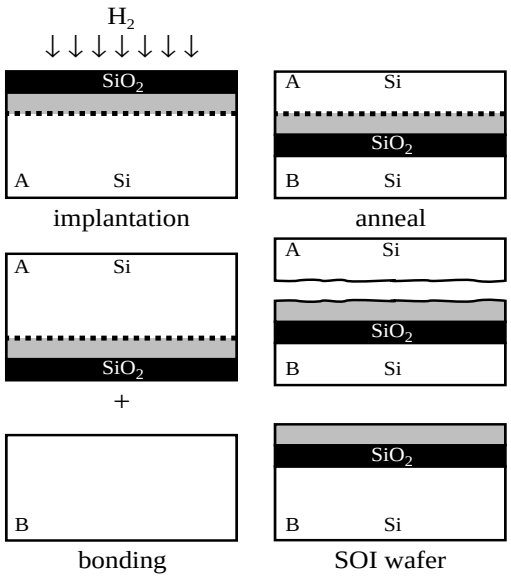

Fig. 3. Synthesis of Unibond wafers.

[3]. Even thick WB films may be useful for sensors and high-voltage devices.

C. Unibond

The leading SOI materials, namely SIMOX and wafer bonding, offer a high-quality crystal, but are limited by a small volume production and a relatively high cost. These problems can be alleviated by the novel *Unibond* material, fabricated with the *Smart Cut* process [4]. There are 6 basic steps (Fig. 3) : (1) thermal oxidation of seed wafer A, defining the BOX thickness (10 nm–1.5 μm), (2) deep implantation of hydrogen (2–10 $\times 10^{16}\,cm^{-2}$) into wafer A to locate the splitting region (the thickness of the Si film, up to 1.2 μm, is selected by tuning the implant energy), (3) bonding of wafer A to a handle wafer B, (4) anneal-induced subsurface cleavage of wafer A (*i.e smart-cut*: the thin SOI film, separated from wafer A, remains bonded to wafer B), (5) high-temperature annealing (1100°C) to improve the bonding, and (6) touch polishing to erase the roughness of the top silicon surface.

Final thickness uniformity is better than ±5 nm and the roughness is below 0.15 nm RMS. The Unibond structure exhibits a very low dislocation density, excellent electrical properties, and no oxide defects [5]. Note that the rest of wafer A is recycled as a 'new' wafer B.

D. Other SOI Technologies

FIPOS — This technology (FIPOS: Full Isolation by Porous Oxidized Silicon) makes use of oxidized porous silicon. In a typical FIPOS sequence, phosphorus islands are implanted in a p-type Si wafer. Anodic reac-

tion in HF converts the superficial p-type regions into porous silicon, whereas the n-type islands are not affected. Porous Si has a very large surface/volume ratio (200–1000 m^2 per cm^3) and is selectively oxidized. The main expectation comes from the possible application of electroluminescence in SOI, whereas the disadvantage is that FIPOS involves a wet process.

ZMR — A thermal oxide (0.2–2 μm thick BOX) is first grown on a silicon substrate, followed by deposition of a poly-Si film. The Zone Melting Recrystallization (ZMR) is achieved by scanning a source of energy (lamp, graphite strip heater, electron beam, laser) across the film [1]. The ZMR process can be unseeded or seeded, the latter being subject to thermal and topological discontinuities. Surface uniformity can be recovered by planarization and thinning. The predominant defects that hamper the wide application of ZMR are grain subboundaries. The ZMR process is envisaged mostly for 3–D integrated circuits (located in 'defect-free' islands) with multifunctional operation, parallel processing and optical sensing functions.

SOS — The epitaxial growth of Si films on Al_2O_3 gives rise to small silicon islands that eventually coalesce. The standard Silicon on Sapphire (SOS) film suffers from lateral stress, in-depth inhomogeneity, and defective interface transition layer [1], but can be improved by *solid-phase epitaxial regrowth*. Silicon ions are implanted to amorphise the film and erase the memory of the damaged lattice and interface. Annealing allows the epitaxial regrowth of the film, starting from the 'seeding' surface [6]. Recently, 100 nm thick SOS films with good quality have been grown on 6–8" wafers.

III. Typical SOI Devices

A. High Voltage Devices

Lateral DMOS transistors with long drift region have been fabricated on standard SIMOX whereas vertical DMOS can be accommodated in thicker wafer-bonding SOI [1]. Interrupted SIMOX process (Fig. 2d) offers the possibility to synthesize locally a buried oxide. Therefore, a vertical power device (DMOS, IGBT, UMOS, etc), located in the bulk region of the wafer, can be controlled by a low-power CMOS/SOI circuit. An example of 600 V/25 A, smart-power device with 'mezzanine' structure is shown in Fig. 4 [7]. Double SIMOX (Fig. 2c) has also been used.

B. Innovative Devices

The feasibility of 3–dimensional circuits has been demonstrated on ZMR structures. An image signal processor is organized in 3 levels: photodiode arrays in the upper SOI layer, fast A/D converters in the intermediate SOI layer, and arithmetic units and shift registers in the bottom bulk Si level [8]. SOI is also an ideal material for integrated microsensors because the Si/BOX interface gives a perfect etch-stop mark, making it possible to control the fabrication of very thin membranes. A typical pressure sensor is shown in Fig. 5a. Transducers for detection of the magnetic field, gas flow, temperature, radiation, etc, have successfully been integrated on SOI [1].

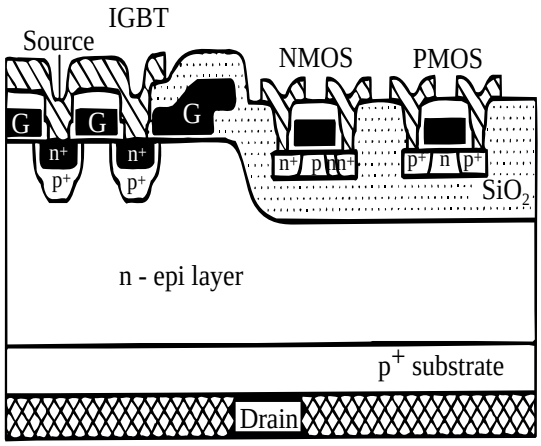

Fig. 4. 600 V/25 A, intelligent vertical IGBT with CMOS control on mezzanine SIMOX structure [7].

The *Gate–All–Around* (GAA) transistor of Fig. 5b makes use of the concept of *volume inversion* (inverting the top and bottom interfaces causes the whole film to be inverted) [9]. The GAA is fabricated by etching a cavity into the BOX and wrapping the transistor body into a poly-Si gate [10]. A similar device is the Delta transistor [11].

The family of SOI devices also includes optical waveguides and modulators, microwave transistors integrated on very high resistivity SIMOX, twin-gate MOSFETs, and other unusual components [1], [10].

C. CMOS Circuits

The superior performance of CMOS circuits on SOI has been repeatedly demonstrated on submicron devices, including ring oscillators, test circuits, A/D converters, microprocessors, SRAM and DRAM memories, etc. It is admitted that the generation (n) on SOI performs comparably well as the *next* generation ($n+1$) on bulk Si.

The device characteristics are compatible with low-voltage/low-power and high speed ULSI applications. Quarter-micron ring oscillators show delay times of 14 ps/stage at 1.5 V [12] and of 45 ps/stage at 1 V [13]. PLL operated at 2.5 V and 4 GHz dissipate 19 mW only [13]. A 1 Gbit DRAM with 1 V supply has been recently presented [14].

Minimum size MOSFETs have been tentatively fabri-

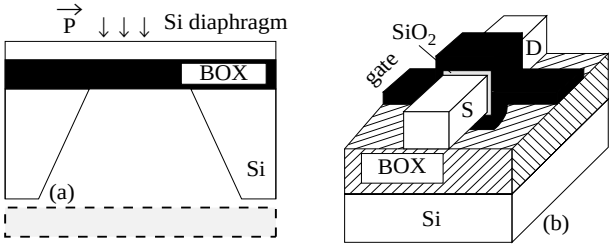

Fig. 5. (a) Pressure microsensor on SOI and (b) Gate–All–Around transistor.

cated: 70 nm length, 10 nm width, and only 2 nm thickness [15]. When these features will be cumulated in a single transistor, the total volume will be as low as $10^{-18}\,\mathrm{cm}^{-3}$! This implies that there will be less than 10^5 Si atoms in the film and the doping will be provided by a unique impurity, whose location will become relevant.

IV. MOSFET Operation

In an SOI–MOSFET (Fig. 1), inversion channels are activated at either the front interface (by biasing the gate V_{G_1}) or at the back interface (by applying a substrate, back-gate voltage V_{G_2}). There are 2 types of SOI transistors: *partially-depleted*, when the depletion layer does not extend from one interface to the other, and *fully-depleted*, when the film is very thin and/or low doped. The confinement of the thin Si film between two oxides and the dual channel operation are responsible for interesting physical mechanisms [1] that are unknown in bulk Si devices.

A. Partially–Depleted SOI MOSFETs

The standard $I_D(V_D, V_G)$ relations existing for bulk Si MOSFETs apply, without any major modification, to partially-depleted SOI transistors provided they have a contact to the Si film (5–terminal devices). Although the back gate bias acts as an extra experimental parameter, its practical influence is rather limited.

If the body contact is missing, the transistor operation is affected by the *floating-body* effects. Majority carriers, created by impact ionization, cannot escape from the film since there is no substrate current. They induce an increase in the body potential which lowers the threshold voltage and gives rise to a kink in the $I_D(V_D)$ characteristics. In short-channel, thin-film SOI MOSFETs, the source-body junction (*i.e* emitter-base junction) is easily turned on: the activation of the inherent lateral bipolar transistor leads to early breakdown and current flow in the film volume. In weak inversion and for high drain bias, the feedback loop (more carriers—more impact ionization events—higher body potential) causes negative resistance regions, hysteresis in $I_D(V_G)$ curves, and eventually latch (loss of gate control) to occur.

Drain current transients are also due to the body isolation. After switching the front and/or back gate bias, there is no substrate current to promptly adjust the majority carrier density: equilibrium is reached through a 'long' generation-recombination process. The 'static' $I_D(V_G)$ characteristics and circuit performance may be affected by the direction of voltage scanning, hold time and delay time. For example, a current *overshoot* is observed when the gate is turned on. The majority carriers, expelled from the depletion region, collect in the neutral region and temporarily increase the body potential (*i.e* lower threshold voltage). Carrier recombination is needed to remove the excess majority carriers giving rise to a transient current reduction. A reciprocal *undershoot* occurs when the gate is switched from strong inversion to weak or moderate inversion. The drain current increases gradually with time as the majority carrier generation allows the depletion region to shrink.

A different problem is *self-heating*. The cooling of SOI transistors is inhibited by the poor thermal conductivity of the surrounding SiO_2 layers. This self-heating essentially results in a reduction of the carrier mobility, a shift in the threshold voltage and an overall negative differential conductance for high gate and drain voltages.

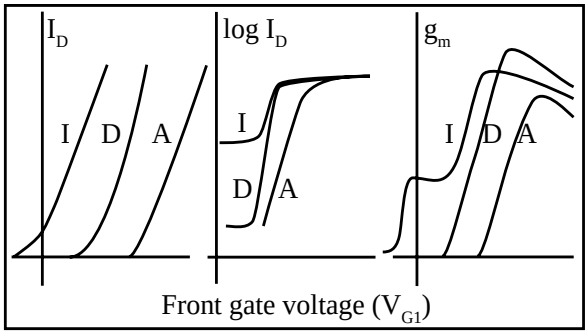

Fig. 6. Generic front-channel characteristics (strong inversion current, weak inversion current and transconductance) of a fully-depleted SOI MOSFET for accumulation (A), depletion (D) and inversion (I) at the back interface.

B. Fully-Depleted SOI MOSFETs

These devices are naturally kink-free, although a reminiscent floating-body effect may still be observed in weak inversion. In fully-depleted SOI MOSFETs, the depletion charge cannot extend with gate bias, therefore the front and back surface potentials become interrelated via a coupling factor roughly equal to the thickness ratio of front and back oxides t_{ox_1}/t_{ox_2}. The apparent properties of one channel vary remarkably with

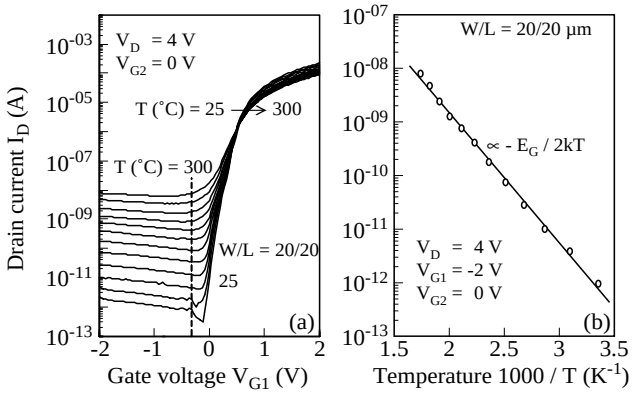

Fig. 7. (a) Subthreshold characteristics in a fully-depleted SOI MOSFET and (b) Arrhenius plot of the leakage current.

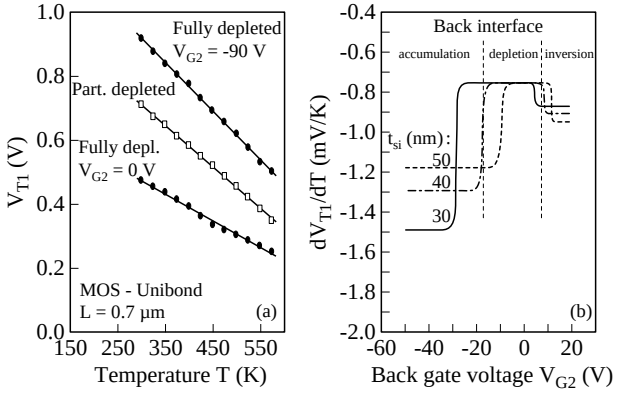

Fig. 8. (a) Threshold voltage versus temperature and (b) threshold reduction rate with temperature versus back gate bias and film thickness in fully-depleted SOI MOSFETs.

the bias of the opposite gate. *Interface coupling* means that front gate measurements are all reminiscent of the bias and quality of the buried interface and oxide.

Totally new $I_D(V_G)$ relations hold in fully-depleted MOSFETs, whose behavior is more complex as it depends on both gate biases. The main transistor characteristics are schematically represented in Fig. 6 and will be discussed next, as a function of the operation temperature.

V. SOI–MOSFET Parameters at High Temperature

A. Leakage Current

Typical subthreshold $I_D(V_G)$ characteristics of an n-channel SOI–MOSFET are shown in Fig. 7a. The off-state leakage current increases exponentially with temperature. The activation energy, deduced from the Arrhenius plot of Fig. 7b, is close to $E_G/2$ and unambiguously indicates a prevailing thermal carrier generation [16]. For proper device operation, the ratio between the on-state and off-state currents must exceed several decades. Since the MOSFET body is very thin, the leakage current in SOI is orders of magnitude lower than in bulk Si transistors. This implies that the ultimate temperature at which a CMOS circuit can still be operated is much higher in SOI. For example, Figure 7a shows that even at 300°C, the I_{on}/I_{off} ratio reaches 4 decades.

B. Threshold Voltage

For successful operation at increasing temperatures, it is important to limit the threshold voltage lowering. This condition is more easily fulfilled in fully-depleted SOI–MOSFETs ($dV_T/dT \simeq -0.7\,\mathrm{mV/K}$ for $V_{G_2} = 0\,\mathrm{V}$, Fig. 8a), where the depletion charge is a constant. However, due to interface coupling, the front channel threshold voltage $V_{T_1}^{dep}$ is not a constant and decreases with the back gate bias V_{G_2}, from accumulation to inversion at the buried interface [17]:

$$V_{T_1}^{dep} = V_{T_1}^{acc} - \frac{C_{si}C_{ox_2}\left(V_{G_2} - V_{G_2}^{acc}\right)}{C_{ox_1}(C_{ox_2} + C_{si} + C_{it_2})} \qquad (1)$$

where C_{si} is the fixed capacitance of the fully-depleted film and $V_{T_1}^{acc}$ is the threshold voltage when the back interface is accumulated

$$V_{T_1}^{acc} = \Phi_{fb_1} + \frac{C_{ox_1} + C_{si} + C_{it_1}}{C_{ox_1}} 2\Phi_F - \frac{Q_{si}}{2C_{ox_1}} \qquad (2)$$

For higher temperatures, the flat-band voltage variation is dominated by the lowering of the Fermi potential and, at a lesser degree, by the bandgap narrowing [18]. The computed curves of Fig. 8b show that the reduction rate of the threshold voltage with temperature is always a minimum for depletion ($V_{G_2} \simeq 0\,V$) and a maximum for accumulation at the back interface. The film thickness shows contrasting effects for accumulation and inversion at the back interface.

Attention is called on the complexity of Eq.(1) as compared to the simpler case of partially-depleted SOI–MOSFETs where the threshold voltage takes the same form as in bulk Si:

$$V_{T_1} = \Phi_{fb_1} + \left(1 + \frac{C_{it_1}}{C_{ox_1}}\right) 2\Phi_F + \frac{\sqrt{4q\epsilon_{si}N_A\Phi_F}}{C_{ox_1}} \qquad (3)$$

There is no back gate dependence, but the temperature sensitivity of the threshold voltage is substantially degraded ($dV_T/dT \simeq -1.2\,\mathrm{mV/K}$, Fig. 8a), mainly because of the variation of the depletion charge with temperature.

A more subtle effect occurs in short-channel SOI–MOSFETs, where the temperature sensitivity is increased (-0.82 mV/K for $V_{G_2} = 0\,\mathrm{V}$). This is due to a *barrier lowering* at the back interface, induced

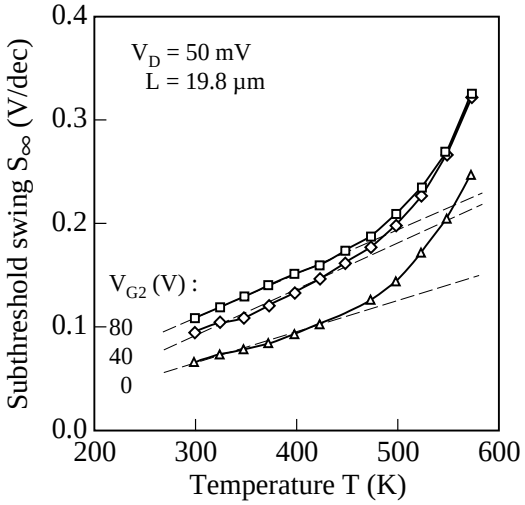

Fig. 9. Subthreshold swing versus temperature in a long, fully-depleted, p-channel SOI MOSFET.

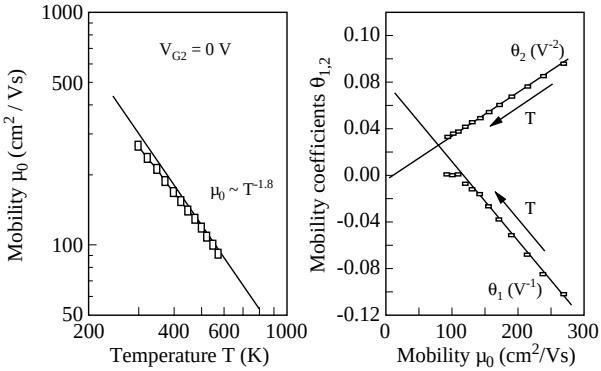

Fig. 10. (a) Low-field mobility versus temperature and (b) mobility attenuation coefficients in a long n-channel SOI MOSFET ($V_{G_2} = 0\,\mathrm{V}$, $V_D = 50\,\mathrm{mV}$).

by the proximity of the source and drain [19]. The back interface status changes from depletion (minimum $|dV_T/dT|$ shift) to weak inversion (higher $|dV_T/dT|$ shift). The same pattern is also observed for p-channel SOI–MOSFETs. However, since they usually have accumulation-mode structure ($P^+P^-P^+$), the current can also flow in the body causing a degraded temperature sensitivity.

C. Subthreshold Slope

The subthreshold *swing* S is proportional to the temperature [1]:

$$S = \left(\frac{d\log_{10} I_D}{dV_G}\right)^{-1} = 2.3\frac{kT}{q}\left(1 + \frac{C_{it_1}}{C_{ox_1}} + \alpha_1\frac{C_{si}}{C_{ox_1}}\right) \tag{4}$$

In partially-depleted MOSFETs, $\alpha_1 = 1$ and $C_{si} = C_d$, whereas in fully-depleted SOI MOSFETs the interface coupling coefficient, $\alpha_1 = (C_{ox_2} + C_{it_2})(C_{si} + C_{ox_2} + C_{it_2})^{-1}$, is lower than unity [20]. This is why the swing approaches the theoretical limit of 60 mV/decade at 300 K. Accumulation at the back interface does decouple the front inversion channel from back interface defects but, in turn, makes α_1 tend to unity, causing an overall degradation of the swing (Fig. 6b).

The temperature dependence of the swing (Fig. 9) shows two distinct regions: a linear variation, corresponding to Eq.(4), and above 175°C an exponential variation arising from the thermal activation of the leakage current [19]:

$$S = S_{lin} + A\exp\left(-\frac{E_G}{2kT}\right) \tag{5}$$

In short-channel fully-depleted MOSFETs, the barrier lowering at the back interface results in a parasitic current which further degrades the swing [19].

The gradual deformation of transconductance curves (Fig. 6c) is due to the influence of the back gate bias which governs the front channel threshold voltage and activates a back inversion channel. The position of the transconductance peak is laterally shifted following the variation of $V_{T_1}(V_{G_2})$ [21]. An unusual situation occurs when the rise in V_{G_1} first opens the *back* channel because the back threshold voltage decreases. The plateau of the front-channel transconductance is a direct measure of the back-channel mobility.

D. Carrier Mobility

For SOI–MOSFET operation in strong inversion and ohmic region, the drain current is expressed as

$$I_D = \frac{C_{ox_1} W V_D}{L}\cdot\frac{\mu_0(V_{G_1} - V_{T_1}(V_{G_2}))}{1 + \theta_1(V_{G_1} - V_{T_1}) + \theta_2(V_{G_1} - V_{T_1})^2} \tag{6}$$

Remark that in Eq.(6), the *field-effect* mobility depends on the low-field mobility μ_0 of front channel carriers, attenuated by the coefficients $\theta_{1,2}$. Such an empirical formulation has the advantage of being well adapted for parameter extraction [22] and circuit design. Nevertheless, it has rigorously been demonstrated that direct relations exist between these 'empirical' coefficients and the 'physical' parameters of the dominant scattering mechanisms (acoustic phonons, ionized impurities, and surface roughness) [23].

The low-field mobility, essentially dominated by phonon scattering above 300 K, decreases rapidly at higher temperature: $\mu_0 \sim T^{-n}$, with $n = 1.8$ (Fig. 10a). In long-channel MOSFETs, the linear attenuation coefficient θ_1 is negative whereas, in short-channels, it is positive and proportional with the series resistance; the negative value of θ_1 becomes smaller for increasing temperature. The quadratic attenuation coefficient

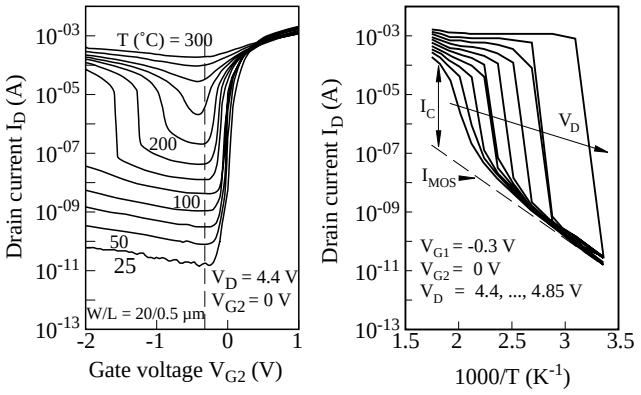

Fig. 11. (a) Subthreshold characteristics showing the temperature-activated latch in a fully-depleted SOI MOSFET and (b) Arrhenius plot of the drain current.

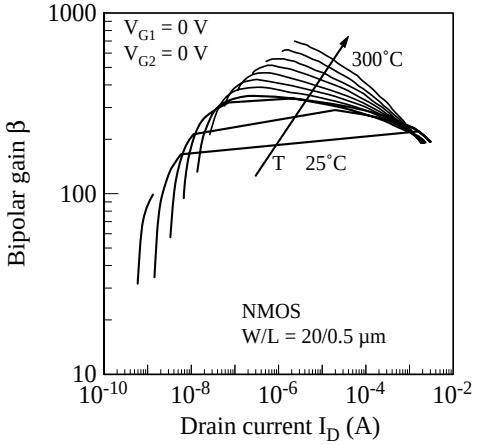

Fig. 12. Bipolar gain versus drain current for different temperatures in a fully-depleted SOI MOSFET.

$\theta_2 > 0$ is dominated by surface roughness scattering, except at high temperature where phonon scattering can make it become slightly negative [24]. Both θ_1 and θ_2 have quasi-linear variations with the low-field mobility μ_0 (Fig. 10b).

VI. Parasitic Bipolar Transistor

The parasitic bipolar transistor (PBT) limits the maximum operation voltage and temperature of short-channel SOI–MOSFETs. The total drain current I_D, the base current I_B and the pure MOS-channel current I_{MOS} are inter-related:

$$I_B = (M-1)I_D, \quad I_D = \beta I_B + I_{MOS} = \frac{I_{MOS}}{1-\beta(M-1)} \tag{7}$$

The latch condition, $\beta(M-1) = 1$, is achieved at high V_D (increased impact-ionization multiplication factor $(M-1)$) or at high temperature (increased gain β).

The temperature activation of the transistor latch, above 200°C, is demonstrated in Fig. 11a. Since bipolar action is more substantial for low V_G, when I_{MOS} is simply the leakage current, it is possible to determine β, as a function of V_D and T, from Eq.(7) : I_D is measured (Fig. 11a), the leakage current $I_{MOS} \sim \exp(-E_A/kT)$ is extracted from the Arrhenius plot (Fig. 11b), and M is computed from standard model [16]. Figure 12 shows that the gain increases initially with temperature and then, as soon as the transistor latches, remains roughly constant. At low current levels, β increases with V_D since the carrier recombination within the base becomes less important. At high injection levels, the minority carrier concentration reaches the doping level and causes β to drop. These results have been confirmed by an independent extraction method [25]. To further validate the data, note that the behavior of β corresponds well with those of the base transport factor and emitter efficiency in Si bipolar transistors.

Two temperature regions can be distinguished. Below 150°C, the bipolar-induced breakdown proceeds in 3 steps. First, β increases with I_D until $\beta(M-1)$ reaches unity. Then, the positive feedback increases I_D instantaneously and brings the device in the high injection level. Finally, β decreases at high I_D and interrupts the feedback mechanism. Above 150°C, the leakage current is high enough to maintain the device in the high injection regime.

In short-channel SOI–MOSFETs, the PBT interacts with other parasitic effects: drain-induced barrier lowering (DIBL), floating body, and self-heating. These mechanisms can be separated by drawing, as in Fig. 13a, the ratio between the output conductance and transconductance versus V_D [18]:

$$\left(\frac{g_D}{g_m}\right)_{sat} = \underbrace{\lambda - \frac{dV_{T,fb}}{dV_D}}_{V_T\ variation} + \underbrace{R_{th}\frac{\partial I_{Dsat}}{\partial T}(V_G - V_T)}_{self\text{-}heating} + \underbrace{\frac{(V_G - V_T)}{1-\beta(M-1)}\frac{\partial \beta(M-1)}{\partial V_D}}_{bipolar} \tag{8}$$

where λ is the DIBL coefficient, $dV_{T,fb}/dV_D$ is the threshold voltage shift due to the residual floating body, R_{th} is the thermal resistance, β is the bipolar gain, and M is the impact ionization multiplication rate.

A remarkable aspect is that, at high temperature, the impact-ionization rate and the subsequent floating body effect are drastically attenuated (for $V_D \simeq 1.5\,\mathrm{V}$ in Fig. 13a); nevertheless, the bipolar action becomes more pronounced (for $V_D \simeq 3\,\mathrm{V}$). After the complete parameter extraction, the $I_D(V_D)$ curves corresponding to the pure MOS transistor can be reconstructed and compared to the experimental characteristics (affected by the bipolar transistor, Fig. 13b).

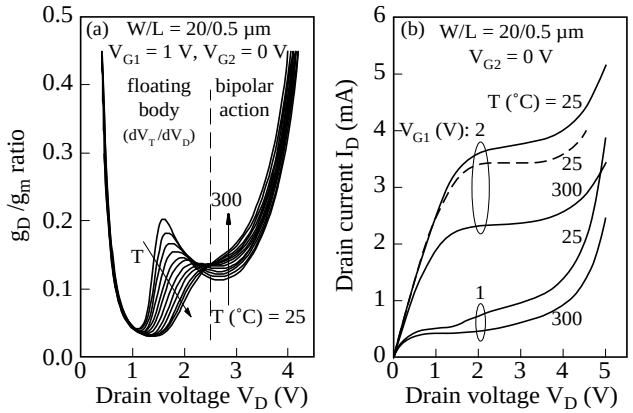

Fig. 13. (a) Conductance-to-transconductance ratio versus drain bias for various temperatures. (b) Experimental $I_D(V_D)$ characteristics at 25°C and 300°C in a fully–depleted SOI MOSFET. The pure, bipolar-free MOS transistor current (dotted curve) was reconstructed after parameter extraction.

VII. Conclusion

The above review of SOI technologies and devices has attempted to demonstrate that SOI has reached a level of maturity which opens new fields of applications. In particular, fully-depleted SOI–MOSFETs stand as the best Si-based devices for operation at high temperature, up to 300–350°C. Their performance, essentially the low leakage current and attenuated shift of the threshold voltage, outperforms bulk Si transistors. However, additional mechanisms have to be accounted for in circuit design and simulation: parasitic bipolar action, floating body, self-heating, and interface coupling including the barrier lowering. The impact of the above mechanisms, except interface coupling, can be minimized by fabricating low-voltage/low-power SOI integrated circuits.

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References

[1] S. Cristoloveanu and S.S. Li, *Electrical Characterization of SOI Materials and Devices*, Kluwer, Norwell (1995).
[2] K. Mitani and U.M. Gösele, *J. Electronic Materials*, vol. 21, p. 669 (1992).
[3] P.B. Mumola, G.J. Gardopee, P.J. Clapis, C.B. Zarowin, L.D. Bollinger, and A.M. Ledger, *IEEE Int. SOI Conf. Proc.*, p. 152 (1992).
[4] M. Bruel, *Electronics Lett.*, vol. 31, 1201 (1995).
[5] D. Munteanu, C. Maleville, S. Cristoloveanu, H. Moriceau, B. Aspar, C. Raynaud, O. Faynot, J–L. Pelloie, and A–J. Auberton–Hervé, *Microelectronic Eng.*, vol. 36, p. 395 (1997).
[6] I. Golecki, in *Comparison of Thin Film Transistor and SOI Technologies*, H.W. Lam and H.J. Thompson eds., North-Holland, Amsterdam, p. 3 (1984).
[7] H. Vogt, *SOI Technology and Devices*, Electrochem. Soc., Pennington, p. 430 (1993).
[8] T. Nishimura, Y. Inoue, K. Sugahara, S. Kusonoki, T. Kumamoto, S. Nakagawa, M. Nakaya, Y. Horiba, and Y. Akasaka, *IEDM Dig.*, p. 111 (1987).
[9] F. Balestra, S. Cristoloveanu, M. Bénachir, J. Brini, and T. Elewa, *IEEE Electron Device Lett.*, vol. 8, p. 410 (1987).
[10] J–P. Colinge, *SOI Technology: Materials to VLSI*, Kluwer, Boston, 1991.
[11] D. Hisamoto, T. Kaga and E. Takeda, *IEEE Trans. Electron Dev.*, vol. 38, p. 1419 (1991).
[12] J. Chen, S. Parke, J. King, F. Assaderaghi, P. Ko, and C. Hu, *IEDM Techn. Dig.*, p. 35 (1992).
[13] T. Tsuchiya, T. Ohno and Y. Kado, *SOI Technology and Devices*, Electrochem. Soc., Pennington, p. 401 (1994).
[14] Y–H. Koh et al, *IEDM Techn. Dig.*, p. 579 (1997).
[15] Y. Ohmura, T. Ishiyama, M. Shoji and K. Izumi, *SOI Technology and Devices*, Electrochem. Soc., Pennington, p. 199 (1996).
[16] D.S. Jeon and D.E. Burk, *IEEE Trans. Electron Devices*, vol. ED–30, p. 1244 (1983).
[17] H-K. Lim and J.G. Fossum, *IEEE Trans. Electron Devices*, vol. ED–30, p. 1244 (1983).
[18] G. Reichert, *PhD Dissertation*, INPG (1998).
[19] G. Reichert, C. Raynaud, O. Faynot, F. Balestra and S. Cristoloveanu, *Microelectronic Eng.*, vol. 36, p. 359 (1997).
[20] B. Mazhari, S. Cristoloveanu, D.E. Ioannou and A.L. Caviglia, *IEEE Trans. Electron Dev.*, vol. ED–38, p. 1289 (1991).
[21] T. Ouisse, S. Cristoloveanu, and G. Borel, *Solid-State Electron.*, vol. 35, p. 141 (1992).
[22] P.K. McLarty, S. Cristoloveanu, O. Faynot, V. Misra, J.R. Hauser, and J.J. Wortman, *Solid-State Electron.*, vol. 38, p. 1175 (1995).
[23] G. Reichert and T. Ouisse, *IEEE Trans. Electron Devices*, vol. ED–43, p. 1394 (1996).
[24] G. Reichert, T. Ouisse, J–L. Pelloie, and S. Cristoloveanu, *Solid-State Electron.*, vol. 39, p. 1347 (1996).
[25] G. Reichert, C. Raynaud, O. Faynot, F. Balestra, and S. Cristoloveanu, *Proc. ESSDERC'97*, Edition Frontières, p. 520 (1997).